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(54) Use of a sacrificial layer to facilitate metallization

(57) A method of fabricating a copper interconnect using a sacrificial layer. A SiC layer (106) is formed over the dielectric layer (102). A sacrificial layer (108) is formed over the SiC layer (106). A trench (112) is etched in the sacrificial layer (108), the SiC layer (106) and the dielectric layer (102). A sputter etch of the sacrificial lay-

er (108) is used to create a wider opening at a top of the sacrificial layer (108) than at a top of the dielectric layer (102). A barrier layer (114) and copper seed layer (116) are formed. The trench (112) is then filled with copper (124). CMP is used to remove the excess copper (124) and barrier layer (114) stopping on the SiC (106).

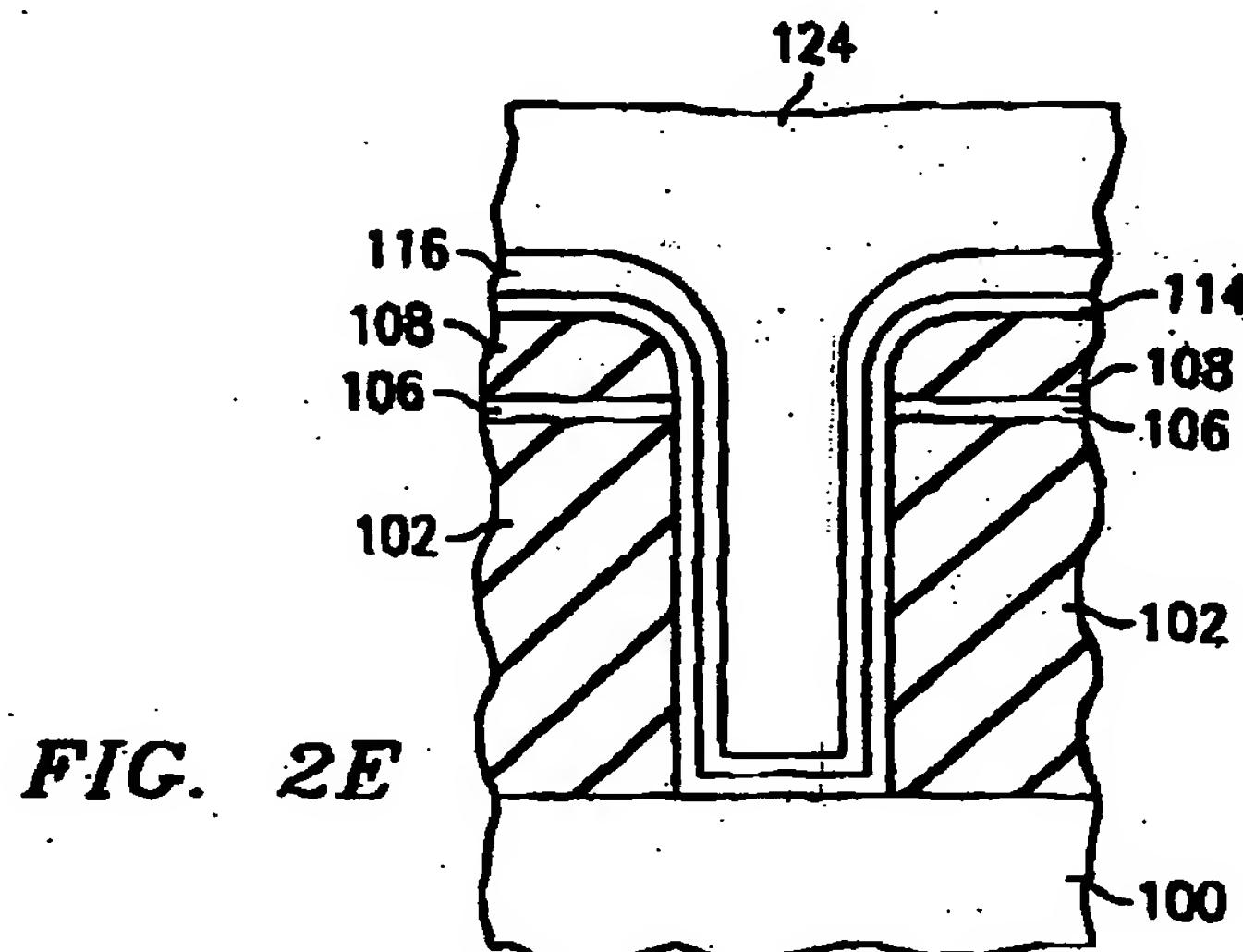


FIG. 2E

Description**FIELD OF THE INVENTION**

[0001] The invention is generally related to the field of fabricating copper interconnects in semiconductor devices and more specifically to the use of a sacrificial layer to facilitate metallization for small features.

BACKGROUND OF THE INVENTION

[0002] As the density of semiconductor devices increases, the demands on interconnect layers for connecting the semiconductor devices to each other also increases. Therefore, there is a desire to switch from the traditional aluminum metal interconnects to copper interconnects. Unfortunately, suitable copper etches for a semiconductor fabrication environment are not readily available. To overcome the copper etch problem, damascene processes have been developed.

[0003] In a conventional interconnect process, the aluminum (and any liner/barrier metals) are deposited, patterned, and etched to form the interconnect lines. Then, an interlevel dielectric (ILD) is deposited and planarized. In a damascene process, the ILD is formed first. The ILD is then patterned and etched. A thin liner/barrier material is then deposited over the structure followed by copper deposition over the liner/barrier material. Then, the copper and liner/barrier material are chemically-mechanically polished to remove the material from over the ILD, leaving metal interconnect lines. A metal etch is thereby avoided.

[0004] The most practical technique for forming copper interconnects is electrochemical deposition (ECD). In this process, after the liner/barrier material is deposited, a seed layer of copper is deposited. Then, ECD is used to deposit copper over the seed layer.

[0005] At this time, the only practical method for forming the copper seed layer is ionized sputtering. However, sputtering is a line-of-sight technique that has poor step coverage. The major problem for a sputtered film is the overhang near the top of the small features. As a result, an overhang 18 of the seed 16 material occurs at the top of a trench or via 12 as illustrated in FIG. 1. During the subsequent copper ECD, the overhang causes premature closing of the trench or via 12, leaving behind seams and/or voids in the copper fill material.

SUMMARY OF THE INVENTION

[0006] The invention is a method of fabricating a copper interconnect using a sacrificial layer. A polish stop layer is formed over a dielectric layer. A sacrificial layer is formed over the polish stop layer. A trench is etched in the sacrificial layer, the polish stop layer, and the dielectric layer. A sputter etch of the sacrificial layer is used to create a wider opening at a top of the sacrificial layer than at a top of the dielectric layer. A barrier layer

and copper seed layer are formed. The trench is then filled with copper. CMP is used to remove the excess copper and barrier layer, stopping on the polish stop layer.

5 **[0007]** An advantage of the invention is providing an improved fill process that eliminates the formation of seams in the fill material.

[0008] This and other advantages will be apparent to those of ordinary skill in the art having reference to the 10 specification in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] In the drawings:

15 FIG. 1 is a cross-sectional view of a prior art liner/barrier/seed process that results in an overhang of material at the top of a trench, via, or contact; and FIGs. 2A-2F are cross-sectional drawings of a copper interconnect structure formed according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

25 **[0010]** The invention will now be discussed in conjunction with a dual damascene copper interconnect process. It will be apparent to those of ordinary skill in the art having reference to this specification that the benefits of the invention may be applied to other metallization processes, such as CVD tungsten, CVD Cu, as well as Cu single damascene fabrication.

[0011] An embodiment of the invention is discussed with reference to FIGs. 2A-2F. A semiconductor body 100 is processed through formation of a dielectric 102,

35 as shown in FIG. 2A. Semiconductor body 100 typically comprises a silicon substrate with transistors and other devices formed therein. Semiconductor body 100 also includes the pre-metal dielectric (PMD), interlevel dielectric (ILD), and may include one or more metal interconnect layers. Suitable dielectrics for dielectric 102, such as silicon dioxides, fluorine-doped silicate glass (FSG), organo-silicate glass (OSG), hydrogen silsesquioxane (HSQ), and combinations thereof, are known in the art. Dielectric 102 is a thick dielectric layer having a thickness in the range of 0.1 um - 1 um.

[0012] Prior to etching trenches (and vias), a polish stop layer 106 is formed over IMD 104. In the preferred embodiment, polish stop layer 106 comprises SiC. Alternative polish stop materials, such as Si₃N₄, are available.

50 The thickness of polish stop layer 106 is in the range of 3-100nm. Polish stop layer 106 should be as thin as possible to minimize the increase in aspect ratio of the trench and still be thick enough to serve as a CMP polish stop.

55 **[0013]** Still referring to FIG. 2A, a sacrificial layer 108 is formed over polish stop layer 106. Sacrificial layer 108 comprises a material with high CMP rate compared to the polish stop layer 106. Suitable materials for the sac-

ificial layer 108 include SiO_2 , SiOF , and OSG . The thickness of sacrificial layer 108 is in the range of 30-200nm.

[0014] In a copper dual damascene process, both the vias and trenches are etched in the dielectric. Referring to FIG. 2B, a trench 112 is etched in dielectric 102. Vias (not shown) are used to connect to underlying metal interconnect layers. Trench 112 is used to form the metal interconnect lines. In a via first process, a via is patterned and etched through sacrificial layer 108, polish stop layer 106, and dielectric layer 102. The via pattern is removed and vias are filled with a BARC material to protect the via during the trench etch. Trench 112 is then patterned and etched through sacrificial layer 108, polish stop layer 106 and dielectric 102. The trench pattern and BARC material are then removed resulting in the structure of FIG. 2B.

[0015] Referring to FIG. 2C, a pre-sputter etch is used to pull back the corners of sacrificial layer 108. Polish stop layer 106 protects the corners of dielectric 102 during the etch. A low bias (with bias voltage in the range of 0-300V) sputter process with Ar gas is preferred to preferentially remove the corner of the sacrificial layer. The extent of the pull back is determined by the amount of the slope needed to offset potential over-hang of subsequently deposited barrier/seed layers. A typical etch time of 20-100sec is used to create the required corner. This process also removes metal oxide of the underlying metal layer, which is beneficial for reducing via resistance.

[0016] Liner/barrier layer 114 is deposited over sacrificial layer 108 and in trench 112 and via 110, as shown in FIG. 2D.

[0017] Liner/barrier layer 114 functions to prevent copper diffusion into the dielectric layer. For example, liner/barrier layer 114 may comprise Ti or TiN. Other suitable liner/barrier materials such as Ta, TaN, TiN, TaNSi, TiNSi, MoN and WN are known in the art. Liner/barrier 114 may be deposited using CVD or PVD processes. However, due to the nature of the PVD process, the thickness of the liner/barrier layer 114 would be greater at the top of sacrificial layer 108 if PVD is used. The wide opening in sacrificial layer 108 will minimize the potential over-hang even when PVD is used.

[0018] In a copper interconnect process, a copper seed layer 116 is deposited over liner/barrier layer 114. Seed layer 116 is deposited using a PVD process. The barrier/seed stack has minimal overhang near the top of trench 112 due to the wide opening in sacrificial layer 108.

[0019] After the seed deposition, copper ECD is performed as shown in FIG. 2E to form copper layer 124. Because the sputter etch removes/reduces the overhang 111, no seam forms in electroplated copper layer 124 due to early closure at the tops of the trench or via. Various copper ECD processes are known in the art. In one example, a 3-step process is used. After placing the wafer in the plating solution, a current of approximately

0.75 Amps is passed through the seed layer 112 for a time on the order of 15 secs. The current is then increased to around 3 Amps for approximately 60 seconds. Final plating occurs at a current of about 7.5Amps with the duration determined by the final desired thickness. A quick spin-rinse dry (SRD) is performed in the plating cell above the plating solution. The wafer is then transferred to the SRD cell and a post-ECD SRD is used to clean the plating residue.

[0020] Processing then continues to chemically-mechanically polish the excess copper layer 124 and 116, liner/barrier 114, and sacrificial layer 108 over the field to form the copper interconnect, as shown in FIG. 2F. Sacrificial layer 108 also provides an advantage during this CMP step. A two-step CMP process is used to accomplish this task: the first CMP step remove the excess Cu on the field and stop on the barrier layer 114. The second CMP step removes barrier 114, along with sacrificial layer 108 and stops at the polish stop layer 106.

[0021] Additional metal interconnect layers may then be formed followed by packaging.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

Claims

- 35 1. A method of fabricating an integrated circuit, comprising the steps of:
 - 36 forming a dielectric layer over a semiconductor body;
 - 37 forming a polish stop layer over said dielectric layer;
 - 38 forming a sacrificial layer over said polish stop layer;
 - 39 forming a hole in said sacrificial layer, said polish stop layer and said dielectric layer;
 - 40 performing a sputter etch of said sacrificial layer;
 - 41 forming a barrier layer over said sacrificial layer and in said hole;
 - 42 depositing a copper seed layer over said barrier layer; and
 - 43 depositing copper to fill said hole.
- 44 2. The method of claim 1, wherein said hole comprises a trench.
- 45 3. The method of claim 1 or claim 2 wherein said polish stop layer comprises SiC .

4. The method of claim 1, claim 2 or claim 3 wherein said sacrificial layer comprises SiO₂.
5. The method of claim 1, claim 2 or claim 3 wherein said sacrificial layer comprises SiOF. 5
6. The method of claim 1, claim 2 or claim 3 wherein said sacrificial layer comprises OSG.
7. The method of any preceding claim, further comprising the step of chemically mechanically polishing said copper, said barrier layer, and said sacrificial layer to form a copper interconnect. 10
8. The method of any preceding claim, wherein said barrier layer comprises a material selected from the group consisting of Ti, TiN, Ta, TaN, WN, TiNSi, TaNSi, MoN. 15
9. The method of any preceding claim, wherein said sputter etch uses a low bias in the range of 0 to -300 volts. 20
10. The method of any preceding claim and wherein the sputter etch pulls-back a top corner of said sacrificial layer. 25
11. The method of any preceding claim and wherein the sputter etch creates a wider opening at a top of said sacrificial layer than at a top of said dielectric layer. 30
12. A method as claimed in claim 11 wherein said wider opening at the top of the sacrificial layer minimizes an overhang of said copper seed layer. 35
13. An integrated circuit formed by the method of any preceding claim.

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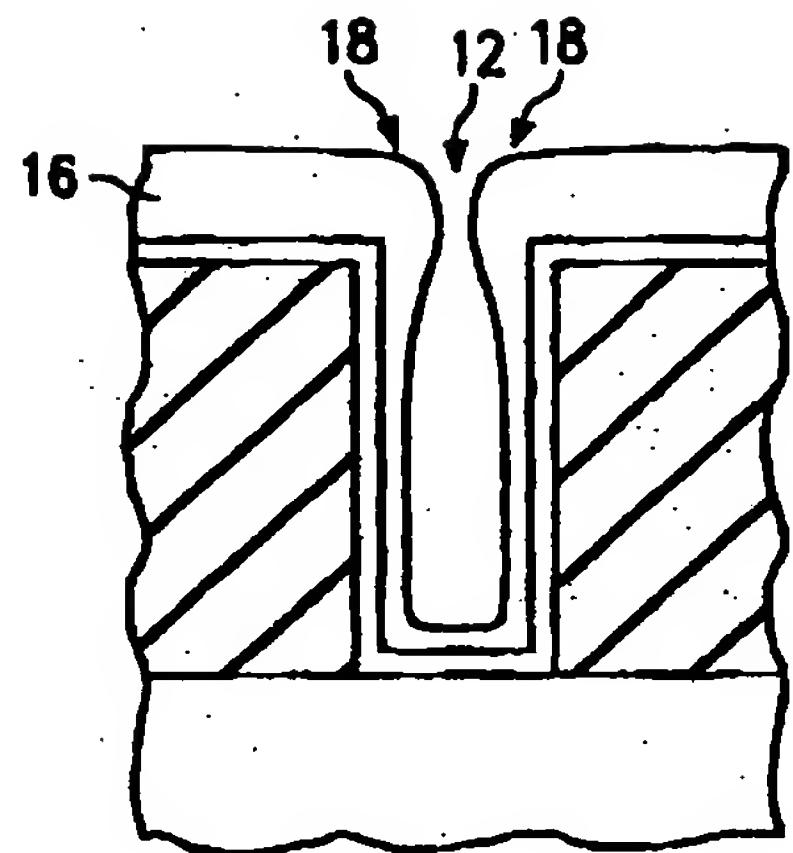


FIG. 1
(PRIOR ART)

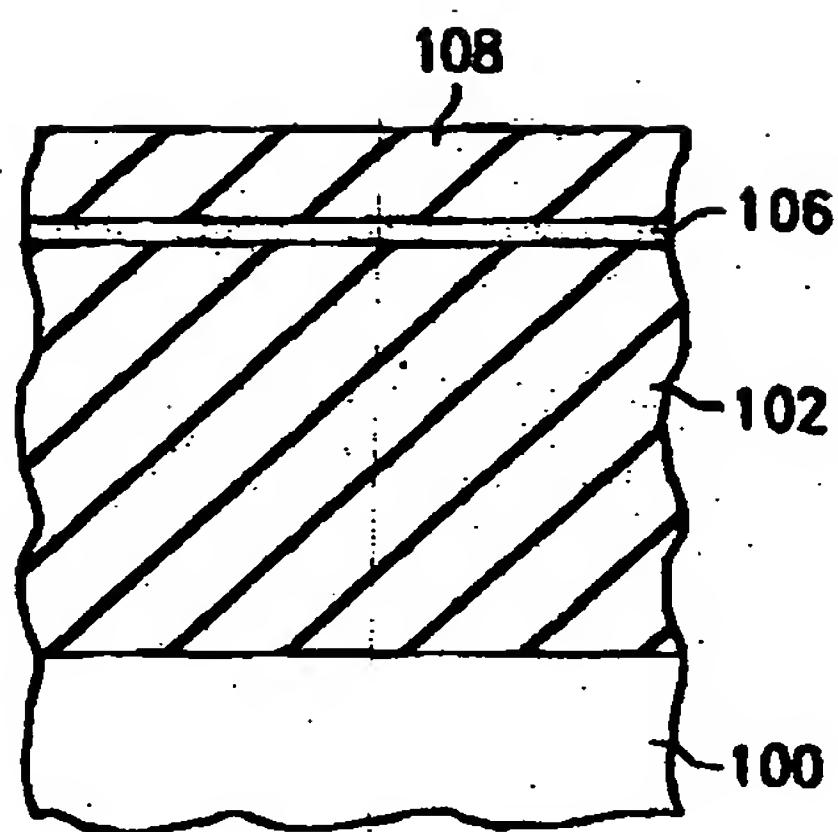


FIG. 2A

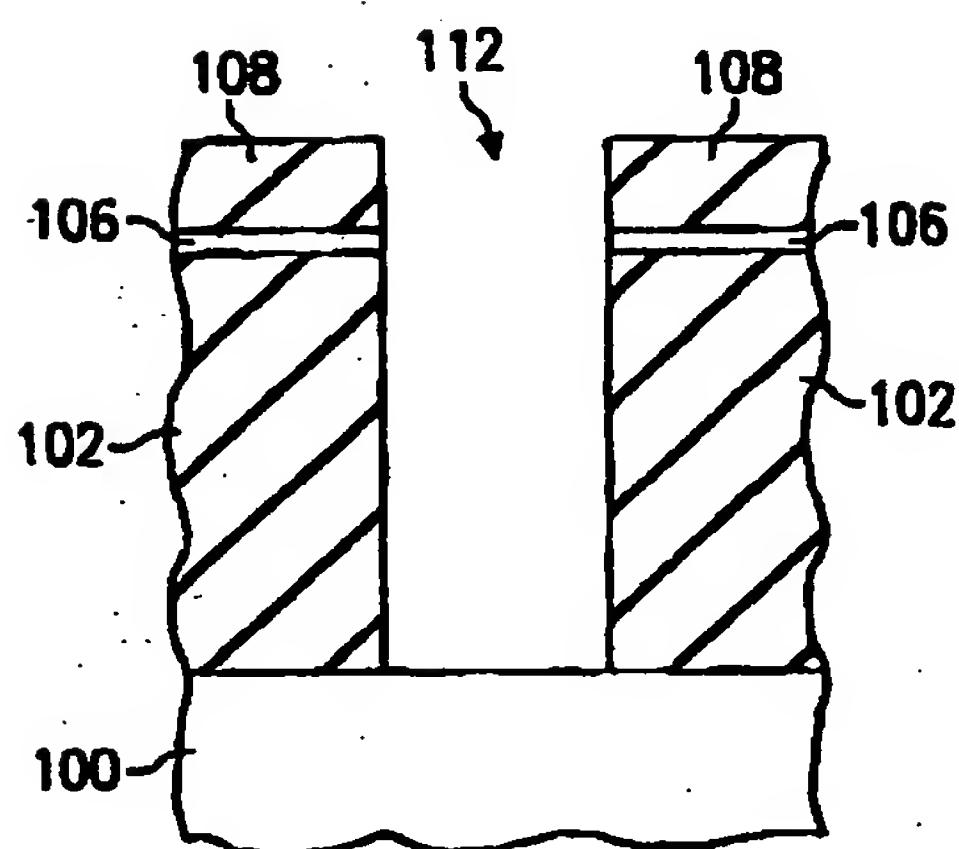


FIG. 2B

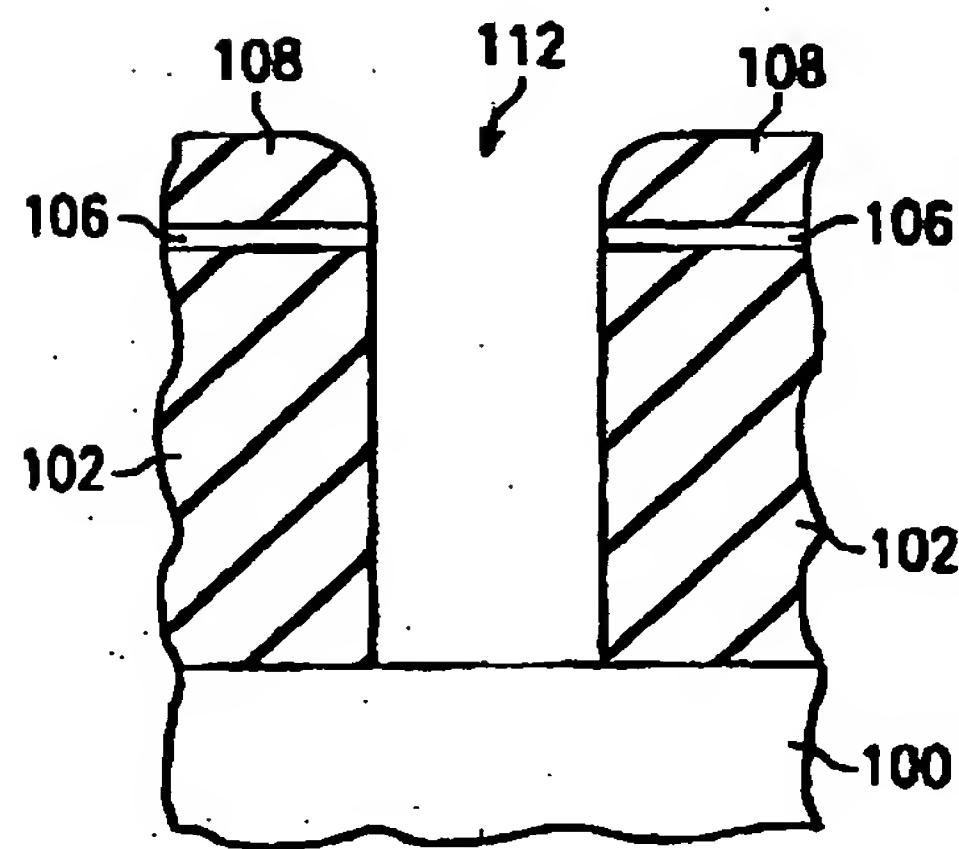


FIG. 2C

